FABRICATING AN EMBEDDED FERROELECTRIC MEMORY CELL

ABSTRACT

Integrated circuit structures comprising an embedded ferroelectric memory cell and methods of forming the same are described. These structures include a transistor level, a ferroelectric device level, a first metal level, an inter-level dielectric level and a second metal level. In a first embodiment, the ferroelectric device level is disposed over an isolation layer of the transistor level and an isolation layer of the ferroelectric level has one or more vias that are laterally sized larger than corresponding contact vias extending through the transistor isolation layer and aligned therewith. In a second embodiment, the first metal level and the ferroelectric device level are integrated into the same level. In a third embodiment, the ferroelectric device level is disposed over the first metal level. In a fourth embodiment, the ferroelectric device level is disposed over the inter-level dielectric level that, in turn, is disposed over the first metal level. In a fifth embodiment, the ferroelectric device level is disposed over the transistor isolation layer and the ferroelectric isolation layer has one or more vias extending through the ferroelectric isolation layer and the transistor isolation layer. These embodiments implement different strategies for improving the yield and performance of embedded ferroelectric devices.